**PATENT**
**29347/597**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (Currently Amended): A semiconductor element comprising:

a substrate;

a first DMOS element formed on a first portion of the substrate, wherein the DMOS element includes:

a source region;

a drain region;

a gate electrode having slanted side walls, a portion of one of the slanted side walls overlapping a part of the source region and another one of the slanted side walls not overlapping the drain region; and

a first MOS element formed on a second portion of the substrate that is separate from the first portion, wherein the first MOS element includes a gate electrode having side walls with a different profile than the slanted side walls of the first DMOS element.

Claim 2 (Cancelled).

Claim 3 (Currently Amended): The semiconductor element of claim 1, wherein the first DMOS element includes:

a well of a first conductive type formed on the substrate;

a body region of a second conductive type formed in the well;

a gate insulating layer formed between the well and the gate electrode;

wherein the ~~a~~ source region comprises ~~of~~ the first conductive type formed in the body region; and

wherein the ~~a~~ drain region comprises ~~of~~ the first conductive type formed in the well and spaced from the source region; ~~and~~.

Claim 4 (Cancelled).

Claim 5 (Original): The semiconductor element of claim 1, wherein the first MOS element includes:

a well of a first conductive type formed on the substrate;

a source region of a second conductive type formed in the well;

a drain region of the second conductive type formed in the well;

a gate electrode formed on the well of the first conductive type; and

a gate insulating layer interposed between the gate electrode and the well of the first conductive type.

Claim 6 (Original): The semiconductor element of claim 1, wherein a gate insulating layer of the first DMOS element includes a relatively thicker portion.

Claim 7 (Amended): The semiconductor element of claim 5, further comprising:

a protection layer covering the first MOS element and the first DMOS element, wherein the protection layer has first and second contact holes that expose the ~~a~~ source region of the first DMOS element and the a-drain region of the first DMOS element, and wherein the protection layer has third and fourth contact holes formed in the protection layer to expose the source region of the first MOS element and the drain region of the first MOS element;

a source electrode that contacts the source region of the first DMOS element through one of the first and second contract holes;

a drain electrode that contacts the drain region of the first DMOS element through the other one of the first and second contact holes;

a source electrode that contacts the source region of the first MOS element through one of the third and fourth contact holes; and

a drain electrode that contacts the drain region of the first MOS element through the other one of the third and fourth contact holes.

Claim 8 (Original): The semiconductor element of claim 1, further comprising:

a second DMOS element formed on the substrate opposing the first DMOS element; and

a second MOS element formed on the substrate opposing the first MOS element.

Claim 9 (Original): The semiconductor element of claim 8, wherein the second DMOS element includes a gate electrode having slanted side walls.

Claims 10-17 (Canceled).